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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/029,583
Filing Date: December 20, 2001
Appellant(s): KAMINS ET AL.

David Collins
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed September 27, 2005 appealing from the Office action mailed May 28, 2004.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,379,572	KIKUCHI ET AL.	4-2002
6,010,831	HATAKEYAMA ET AL.	1-2000

5,900,310	BRANDES ET AL.	5-1999
5,393,373	JUN ET AL.	2-1995
4,407,695	DECKMAN ET AL.	10-1983

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-2, 5, 7, 8, 10-13, 23 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al. (U.S. Pat. 6,379,572) in view of Deckman et al. (U.S. Pat. 4,407,695).

Kikuchi et al. teach in FIGS. 6A & 6B, therein are shown a cross-sectional side view and a top view of ***the insulator 20 (i.e. substrate) (The insulator can be silicon dioxide.*** See Column 4 lines 1-3) and the conductive gate electrode 22 with ***a soft mask material 60*** deposited on the conductive gate electrode 22. ***The soft mask material 60 may be of a number of different materials, such as a silicon nitride (SiN).*** The same numbers are used here to designate the same elements as in the PRIOR ART. Generally there is a cleaning step before deposition of the soft mask material 60 to assure good contact between the soft mask material 60 and the gate electrode 22. (Column 4 lines 57-68)

Referring now to FIGS. 7A & 7B, therein are shown a cross-sectional side view and a top view of the respective structures of FIGS. 6A & 6B ***with microspheres 50-52 deposited on the soft mask material 60.*** Again, the microspheres 51 and 52 are in contact. (Column 5 lines 1-5)

Referring now to FIGS. 8A & 8B, therein are shown a cross-sectional side view and a top view of the respective structures of FIGS. 7A & 7B after ***etching of the soft mask material 60 and before removal of the microspheres 50-52***. During etching of the soft mask material 60, the soft mask material 60 is etched in areas away from the microspheres 50-52 and also undercuts the microspheres 50-52. For example, where the microsphere 50 has a diameter equal to A, the area A under the microsphere 50 will be etched away to have a diameter designated by the letter B. The undercutting leaves soft mask portions 61-63 of the soft mask material 60. As shown in FIG. 8B, the remaining portion soft mask material 60 is removed until a large portion of the conductive gate electrode 22 is exposed. (Column 5 lines 6-19)

Referring now to FIGS. 9A & 9B, therein are shown a cross-sectional side view and a top view of the respective structures of FIGS. 8A & 8B ***after the microspheres 50-52 are removed and a deposition of a hard mask material 64.*** The microspheres 50-52 may be removed by megasonic cleaning or by a process, such as ashing, to burn up the microspheres 50-52 followed by a cleaning process to remove the ash. ***The hard mask material covers the soft mask portions 61-63. The hard mask material 64 may be of a material such as spin-on glass (SOG)***, which is permitted to level out and then is baked to form a hard coating over the soft mask portions 61-63 and the conductive gate electrode 22. (Column 5 lines 20-32)

Referring now to FIGS. 10A & 10B, therein are shown a cross-sectional side view and a top view of the respective structures of FIGS. 9A & 9B ***after chemical mechanical polishing (CMP) to remove the hard mask material 64 until the soft***

mask portions 61-63 are exposed. Alternatively, an etch-back process is used with an etch having selectivity to the soft mask material 60 of the soft mask portions 61-63. FIGS. 10A & 10B also show removal of the soft mask portions 61-63 by isotropic etching to leave the hard mask material 64 with holes 66-68 which expose the conductive gate electrode 22. (Column 5 lines 33-43)

The first mask material can be selected from a group consisting of silicon nitride, silicon oxynitride, and combinations thereof. (Column 6 lines 18-20)

The microspheres can be made of a material selected from silica, glass, plastics, and a combination thereof. (Column 6 lines 30-33)

The second mask can be selected from a material of spun on glass, silicon dioxide and a combination thereof. (Column 6 lines 39-40)

The differences between Kikuchi et al. and the present claims are that utilizing nanoparticles is not discussed and reactive ion etching is not discussed.

Deckman et al. teach directional ion etching to form microcolumnar structures. (See Abstract) Deckman et al. teach coating a substrate with a monolayer of colloidal particles substantially over the entire surface such that the particles are fixed to the substrate in a predetermined way as to particle size distribution and mean distance between particles, the monolayer of colloidal particles serving as an etch mask for forming an etched pattern in the substrate. (Column 8 lines 19-26)

The etching is performed with a reactive plasma with an ion beam. (Column 8 lines 31-38; Column 7 lines 17-19)

Monodispheres in the range of 200 Angstroms ***(i.e. 20 nm)*** to 40 m can be utilized as the mask. (Column 5 lines 7-10) ***(Utilizing the low end of the range will result in Applicant's required nanopore)***

Spheres of 500 Angstroms ***(i.e. 50 nm)*** to 20 microns can be utilized as the mask. (Column 4 lines 35-36) ***(Utilizing the low end of the range will result in Applicant's nanopore)***

The structures to be fabricated can be as small as 50 angstroms. (Column 6 lines 29)

Islands of a silver film can be used as the mask of 50 Angstroms ***(i.e. 5 nm)*** in dimension. (Column 6 lines 40) ***(Utilizing 50 Angstrom mask will result in Applicant's nanopore)***

The motivation for utilizing nanoparticles and reactive ion etching is that it allows deposition of a large are lithographic mask on the surface of a substrate. (Column 2 lines 20-22)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Kikuchi et al. by utilizing nanoparticles of a particular size that will produce holes of a particular size and reactive ion etching as taught by Deckman et al. because it allows for producing a large area lithographic mask on the surface of a substrate.

Claims 3, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al. in view of Deckman et al. as applied to claims 1-2, 5, 7, 8, 10-13, 23 and 47 above, and further in view of Hatakeyama et al. (U.S. Pat. 6,010,831).

The differences not yet discussed are the size of the nanoparticles in the range of 1 to 10 nm is not discussed and the sizes of the holes is not discussed.

Hatakeyama et al. teach utilizing ***nanometer*** or micrometer ***sized microparticles*** to produce a variety of three-dimensional fine structures which have not been possible by the traditional photolithographic technique. An energy beam with reactive gas particle beam can be used to produce the fine structures. (See Abstract)

It is an object of Hatakeyama et al.'s invention to provide a method of energy beam assisted ultra-fine microfabrication to enable fabrication of fine structures in a nanometer range by dispersing micro-particles as beam shielding means on a fabrication surface of a target object. (Column 2 lines 20-24)

The first object is achieved by dispersing and ***position micro-particles having particle sizes in ranges of one of from 1-10 nm***, 2 from 10-100 nm and 2 from 100 nm to 10 micrometers for shielding regions of a fabrication surface of a target object from exposure to an energy beam, and radiating the energy beam on the fabrication surface so as to produce a fine structure by an etching action. (Column 2 lines 41-49)

The target object may be silicon dioxide. (Column 4 lines 27-30)

The width of the fine pattern elements can have a width of 0.1-100 nm. The depth can be between 0.1- 100 nm. (Column 12 lines 61-64)

The motivation for utilizing nanoparticles of a particular size that will produce holes of a particular size is that it allows for reaching dimensions that photolithographic techniques cannot reach. (See Abstract)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized nanoparticles in the range of 1 to 10 nm and developed a particular size of holes as taught by Hatakeyama et al. because it allows for reaching dimensions that photolithographic techniques cannot reach.

Claims 9, 14-20, 24-26, 28-46 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al. in view of Deckman et al. and further in view of Hatakeyama et al. as applied to claims 1-3, 5, 7, 8, 10-13, 21-23 and 47 above, and further in view of Jun et al. (U.S. Pat. 5,393,373).

The differences not yet discussed is utilizing CVD to deposit the insulating material, depositing material in the nanopore, utilizing an electrical substrate of doped polycrystalline silicon, a tunnel barrier and the material being is semiconductive.

Jun et al. teach ***depositing insulation material by CVD***. (Column 6 lines 9-11)

Jun et al. teach in FIGS. 8a to 8e are schematic sectional views for explaining a method of manufacturing capacitors of semiconductor devices in accordance with the second embodiment of the present invention. (Column 6 lines 63-66)

In this method, oxide layer 12 is first coated on semiconductor substrate 11 on which a transistor (not shown) has been previously formed. In oxide layer 12, capacitor node contacts are then formed. Thereafter, ***doped polysilicon layer 24*** is coated on the overall surface of oxide layer 12 to form a plug, as shown in FIG. 8a. ***Insulation layer 25*** such as an oxide layer is then coated on the overall surface of polysilicon layer 24. ***On insulation layer 25, hemisphere particle layer 14 of polysilicon is coated to***

have alternating hills and valleys, as shown in FIG. 8b. (Column 6 lines 67-68; Column 7 lines 1-9)

The portions of insulation layer 25 disposed beneath the valley portions of hemisphere particle layer 14 are then etched back to expose partially polysilicon layer 24, by using the hill portions of hemisphere particle layer 14 as a pattern mask. As a result, insulation layer 25 has a plurality of protrusions thereon, as shown in FIG. 8c. (Column 7 lines 10-16)

Thereafter, ***another doped polysilicon layer 26 is coated on insulation layer 25 to fill valleys thereof and cover the protrusions thereof. Polysilicon layer 26 is then etched back to expose the upper surface of insulation layer 25, as shown in FIG. 8d.*** (Column 7 lines 17-21)

Insulation layer 25 is removed to expose the upper surface of polysilicon layer 24. ***Subsequently, dielectric layer 16 and plate polysilicon layer 17 are coated in turn on the overall upper surface of polysilicon layers 24 and 26 to produce a capacitor, as shown in FIG. 8e.*** (Column 7 lines 23-27)

The motivation for utilizing CVD to deposit the insulating material, depositing material in the nanopore, utilizing an electrical substrate of doped polycrystalline silicon, a tunnel barrier layer and the material being semiconductive is that it allows for production of a semiconductor device.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized CVD to deposit the insulating material, to have deposited material in the nanopore, to have utilized an electrical substrate of

doped polycrystalline silicon, to have utilized a tunnel barrier layer and top have utilized a semiconductive material as taught by Jun et al. is that it allows for production of a semiconductor device.

Claims 4 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al. in view of Deckman et al. further in view of Hatakeyama et al. and further in view of Jun et al. as applied to claims 1-3, 5-26 and 28-48 above, and further in view of Brandes et al. (U.S. Pat. 5,900,301).

The difference not yet discussed is the particle being inorganic coated with an organic.

Brandes et al. teach applying carbon particles for etching. The particles are applied through an organic solvent. (Column 9 lines 21-59)

The motivation for utilizing a particle that is inorganic coated with an organic is that it allows for developing pillars when anisotropic etching takes place. (See Figure 6C)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized a particle being inorganic coated with an organic as taught by Brandes et al. because it allows for the development of pillars when etching.

(10) Response to Argument

(A) RESPONSE TO THE ARGUMENTS TO THE PATENTABILITY OF CLAIMS 1-2, 5, 7, 8, 10-13, 23 AND 47 OVER KIKUCHI ET AL. IN VIEW OF DECKMAN ET AL.:

In response to the argument that Appellants' claimed method does not teach utilizing a uniform packing to form the pores, it is argued that Appellants' claims are silent with regard to the packing style and the claims would be interpreted to read on any packing style available.

In response to the argument that neither Kikuchi et al. nor Deckman et al. teach forming at least one nanopore for aligning at least one molecule therein, it is argued that Kikuchi et al. teach forming a pore on a substrate utilizing steps which are the same as Appellants' step except for the size of the particle used for the mask and the reactive ion etching utilized. Deckman provide the required particle size for forming the pore and the required reactive ion etching. (See Kikuchi et al. and Deckman discussed above)

In response to the argument that Deckman et al. does not teach reactive ion etching, it is argued that Deckman et al. does teach reactive ion etching since Deckman et al. suggest that reactive ion beam milling can be used to etch the substrate. Here ions are used and a reactive gas is used as required by reactive ion etching. (See Deckman et al. discussed above)

(B) RESPONSE TO THE ARGUMENTS OF THE PATENTABILITY OF CLAIMS 3, 21, AND 22 OVER KIKUCHI ET AL. IN VIEW OF DECKMAN ET AL. AND HATAKEYAMA ET AL.:

In response to the argument that there is no suggestion to combine the reference Kikuchi et al. which forms gate emitter openings or voids with the references of Deckman et al. and Hatakeyama et al. which forms solid microcolumnar pillars and

cones, it is argued that it would be obvious to combine the references since all the references produce nanoscale openings.

In response to the argument that utilizing nanoparticles of a particular size does not necessarily result in nanopores of a particular size, it is argued that since the nanoparticles mask nano areas that the resultant etch would produce nanopores. An argument that "not necessarily" producing nanopores is not persuasive since "not necessarily" is open to produces nanopores.

(C) RESPONSE TO THE ARGUMENTS OF THE PATENTABILITY OF CLAIMS 9, 14-20, 24-26, AND 48 OVER KIKUCHI ET AL. IN VIEW OF DECKMAN ET AL., HATAKEYAMA ET AL. AND JUN ET AL.:

(C1) THE PATENTABILITY OF CLAIMS 9 AND 14-20

In response to the argument that since the combination of Kikuchi et al. and Hatakeyama is flawed the combination of Kikuchi et al. with Hatakeyama and Jun et al. is also flawed, it is argued that as discussed above the combination of Kikuchi et al. and Hatakeyama is not flawed and therefore the combination of Kikuchi et al. with Hatakeyama and Jun et al. is not flawed.

(C2) THE PATENTABILITY OF CLAIMS 24-26, 28-46 and 48

In response to the argument that the prior art does not deposit "at least one molecule" in a nanopore, it is argued that at least one molecule could include more than one molecule and the layer would include at least one molecule.

In response to the argument that the prior art of record does not teach molecular electronic devices, it is argued that the prior art of record teach production of semiconductor devices which act to form electronic devices with molecular structures.

In response to the argument that the prior art does not teach tunnel barrier, it is argued that as Appellant admits Jun et al. at least imply barriers. Appellant further points out that there would be a finite probability of tunnelling. This finite probability suggests a tunnel barrier layer.

In response to the argument that Jun et al. do not teach hyperfine patterning to Appellants' range of 1 to 10 nm, it is argued that at least Deckman teach pattering to within Appellants' range. (i.e. 50 nm). (See Deckman discussed above)

(D) RESPONSE TO THE ARGUMENTS OF THE PATENTABILITY OF CLAIMS 4 AND 27 OVER KIKUCHI ET AL. IN VIEW OF DECKMAN ET AL., HATAKEYAMA ET AL., JUN ET AL., AND BRANDES ET AL.:

In response to the argument that the prior art does not teach an inorganic core and organic shell as a unit, it is argued that the claims do not require that the inorganic core and organic shell be a unit and thus Brandes et al. suggest that inorganic core and organic covering. (See Brandes et al. discussed above)

In response to the argument that coating an inorganic core with an organic material does not have anything to do with developing pillars, it is argued that Brandes inorganic core with an organic material relate to particles that can be used as an etch mask and as evidenced by Kikuchi et al. such particles can be used as an etch mask for developing pillars. (See Brandes et al. and Kikuchi et al. discussed above)

(E1) RESPONSE TO THE ARGUMENTS OF THE PATENTABILITY OF CLAIMS 47 AND 48:

In response to the argument the prior art of record does not teach forming nanopores in which each nanopore contains a single molecule, it is argued that depending on the size of the particle used as the etch mask and the coating material that a single molecule could fill the pore. (See Kikuchi et al. discussed above)

(E2) RESPONSE TO THE ARGUMENTS OF HINDSIGHT:

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Rodney McDonald

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PRIMARY EXAMINER

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